FAIRCHILD SEMICONDUCTOR™

May 2000

QFET™

FQS4903

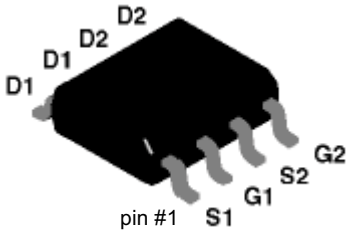
500V Dual N-Channel MOSFET

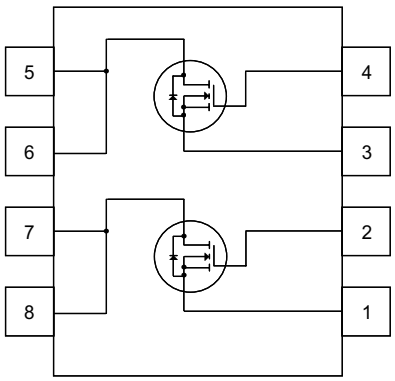
General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switch mode power supply, power factor correction, electronic lamp ballast based on half bridge.

Features

- 0.37A, 500V, $R_{DS(on)}$ = 6.2Ω @V_{GS} = 10 V
- Low gate charge (typical 6.3 nC)
- Low Crss (typical 4.5 pF)
- Fast switching
- Improved dv/dt capability





Absolute Maximum Ratings

T_A = 25°C unless otherwise noted

Symbol	Parameter		FQS4903	Units
V_{DSS}	Drain-Source Voltage		500	V
I_D	Drain Current - Continuous (T_A = 25°C)		0.37	A
	- Continuous (T_A = 70°C)		0.234	A
I_{DM}	Drain Curent - Pulsed	(Note 1)	1.48	A
V_{GSS}	Gate-Source Voltage		± 25	V
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	4.5	V/ns
P_D	Power Dissipation (T_A = 25°C)		2.0	W
	(T_A = 70°C)		1.3	W
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	°C

Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	62.5	°C/W

Electrical Characteristics

T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	500	--	--	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	--	0.49	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 500 V, V_{GS} = 0 V	--	--	1	μA
		V_{DS} = 400 V, T_C = 125°C	--	--	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 25 V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -25 V, V_{DS} = 0 V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 0.185 A	--	4.7	6.2	Ω
g_{FS}	Forward Transconductance	V_{DS} = 35 V, I_D = 0.185 A (Note 3)	--	0.13	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	--	155	200	pF
C_{oss}	Output Capacitance		--	25	35	pF
C_{rss}	Reverse Transfer Capacitance		--	4.5	6.0	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 250 V, I_D = 0.37 A, R_G = 25 Ω (Note 3,4)	--	5.5	20	ns
t_r	Turn-On Rise Time		--	20	50	ns
$t_{d(off)}$	Turn-Off Delay Time		--	20	50	ns
t_f	Turn-Off Fall Time		--	45	100	ns
Q_g	Total Gate Charge	V_{DS} = 400 V, I_D = 0.37 A, V_{GS} = 10 V (Note 3,4)	--	6.3	8.2	nC
Q_{gs}	Gate-Source Charge		--	0.56	--	nC
Q_{gd}	Gate-Drain Charge		--	3.63	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	0.37	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	1.48	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 0.37 A	--	--	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 0.37 A, dI_F / dt = 100 A/μs (Note 3)	--	100	--	ns
Q_{rr}	Reverse Recovery Charge		--	0.175	--	μC

Notes:
1. Repetitive Rating : Pulse width limited by maximum junction temperature
3. $I_{SD} \leq$ 0.37A, di/dt $\leq$ 200A/μs, $V_{DD} \leq BV_{DSS}$, Starting T_J = 25°C
4. Pulse Test : Pulse width $\leq$ 300μs, Duty cycle $\leq$ 2%
5. Essentially independent of operating temperature

Typical Characteristics

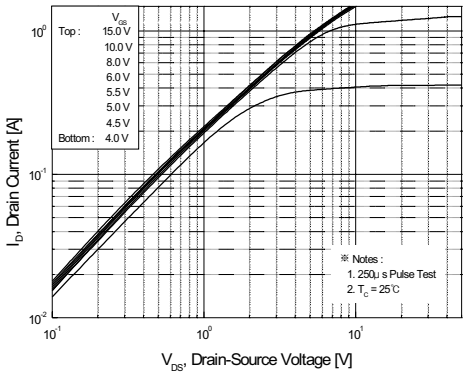


Figure 1. On-Region Characteristics

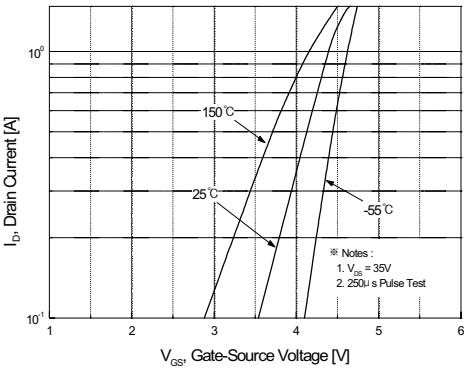


Figure 2. Transfer Characteristics

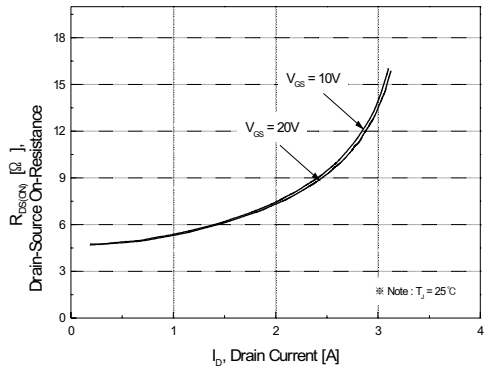


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

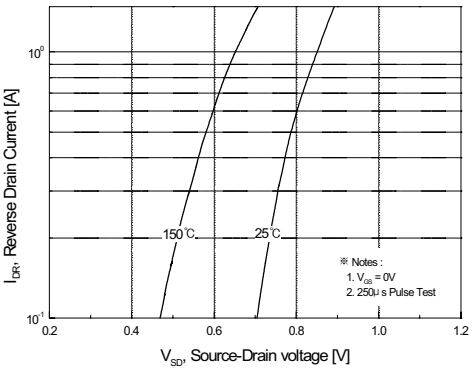


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

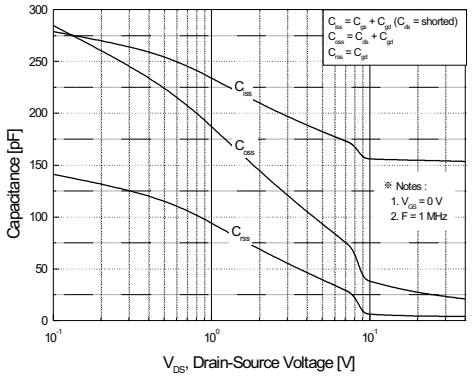


Figure 5. Capacitance Characteristics

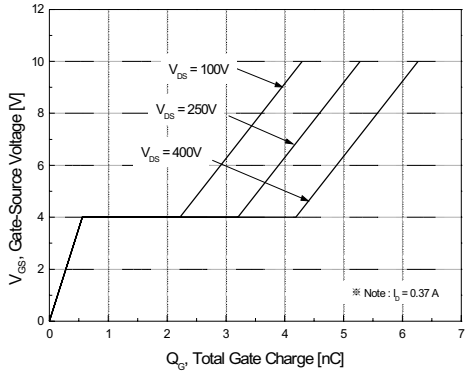


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

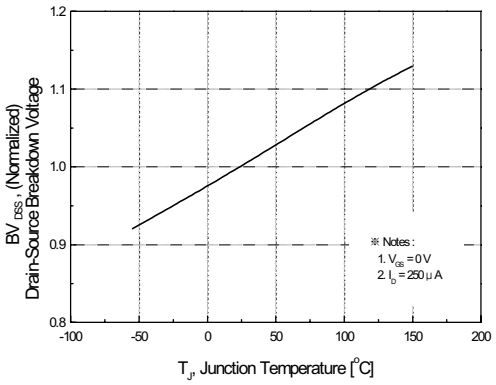


Figure 7. Breakdown Voltage Variation vs. Temperature

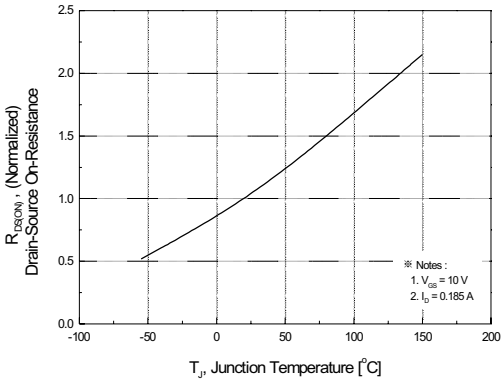


Figure 8. On-Resistance Variation vs. Temperature

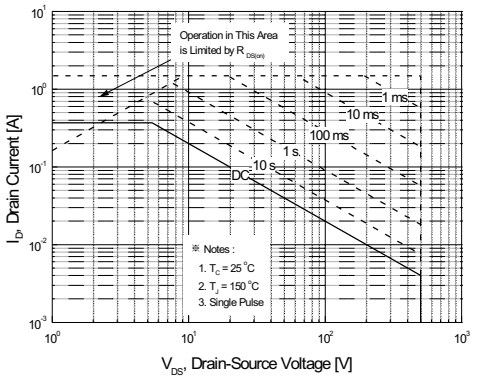


Figure 9. Maximum Safe Operating Area

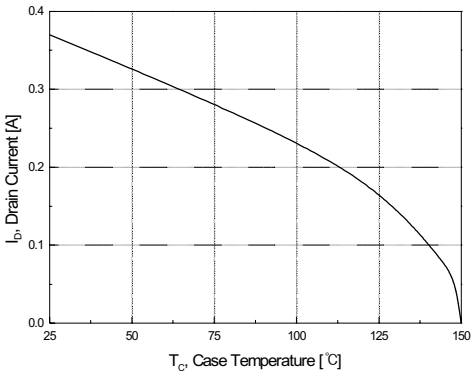


Figure 10. Maximum Drain Current vs. Case Temperature

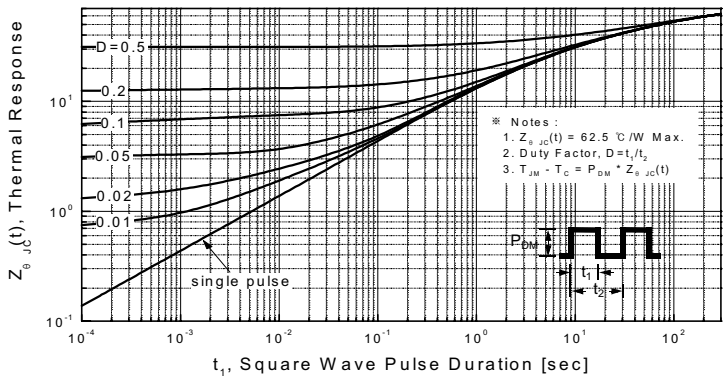
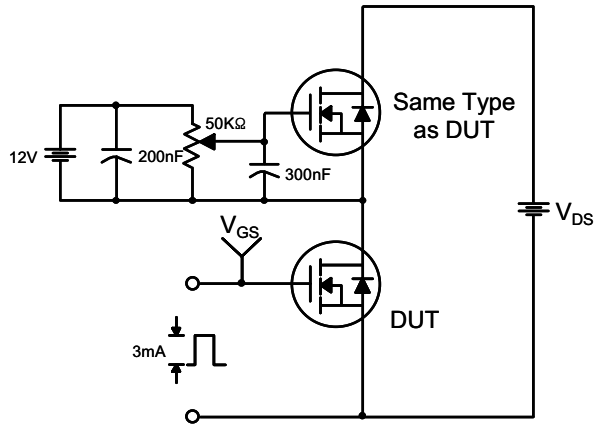
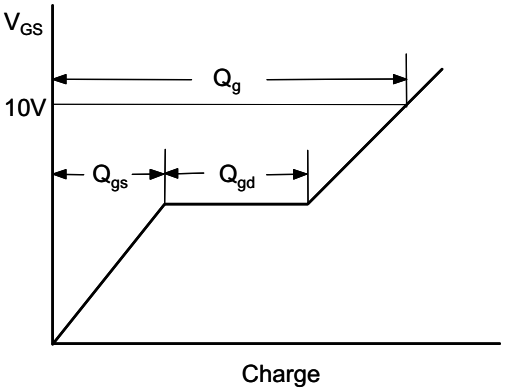


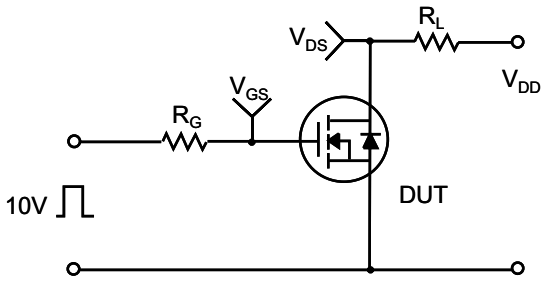
Figure 11. Transient Thermal Response Curve

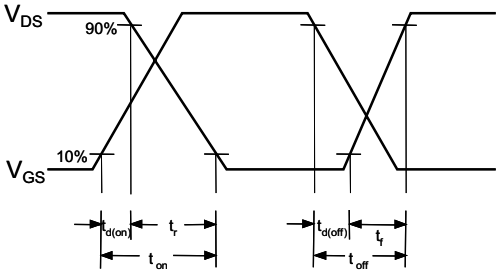
Gate Charge Test Circuit & Waveform



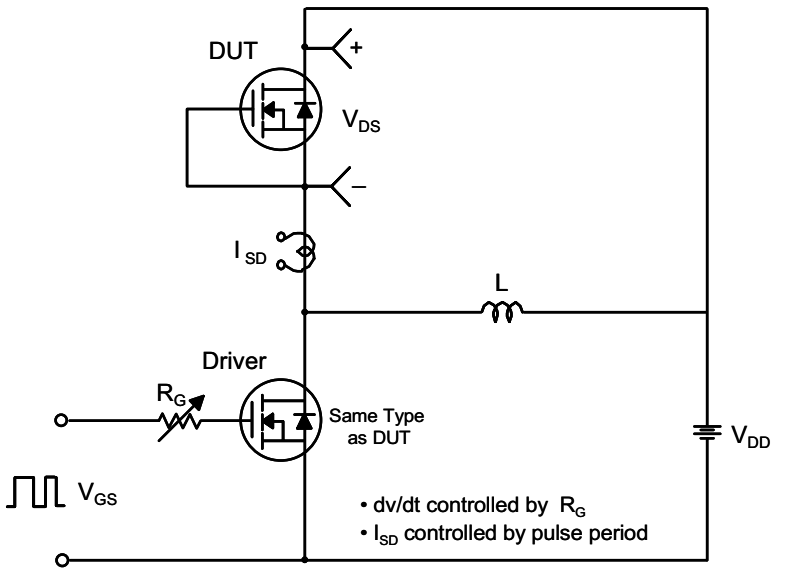


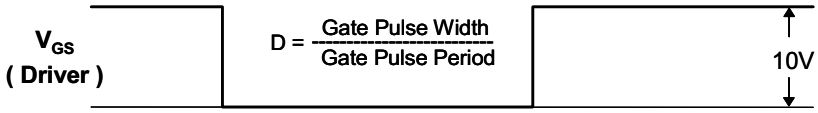
Resistive Switching Test Circuit & Waveforms

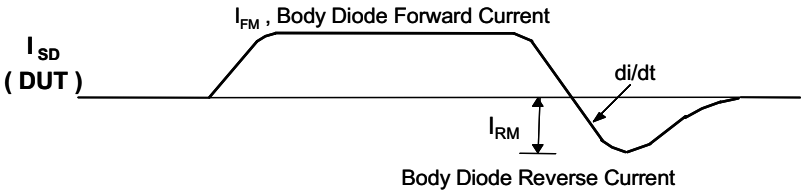


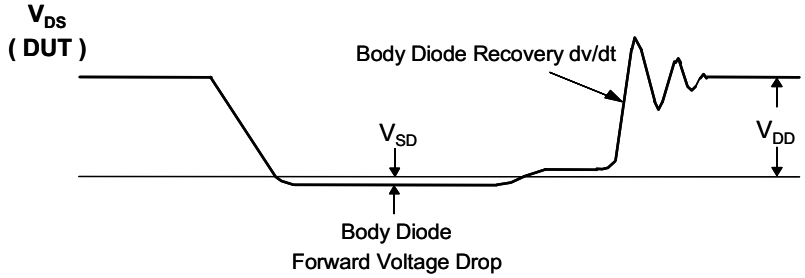


Peak Diode Recovery dv/dt Test Circuit & Waveforms



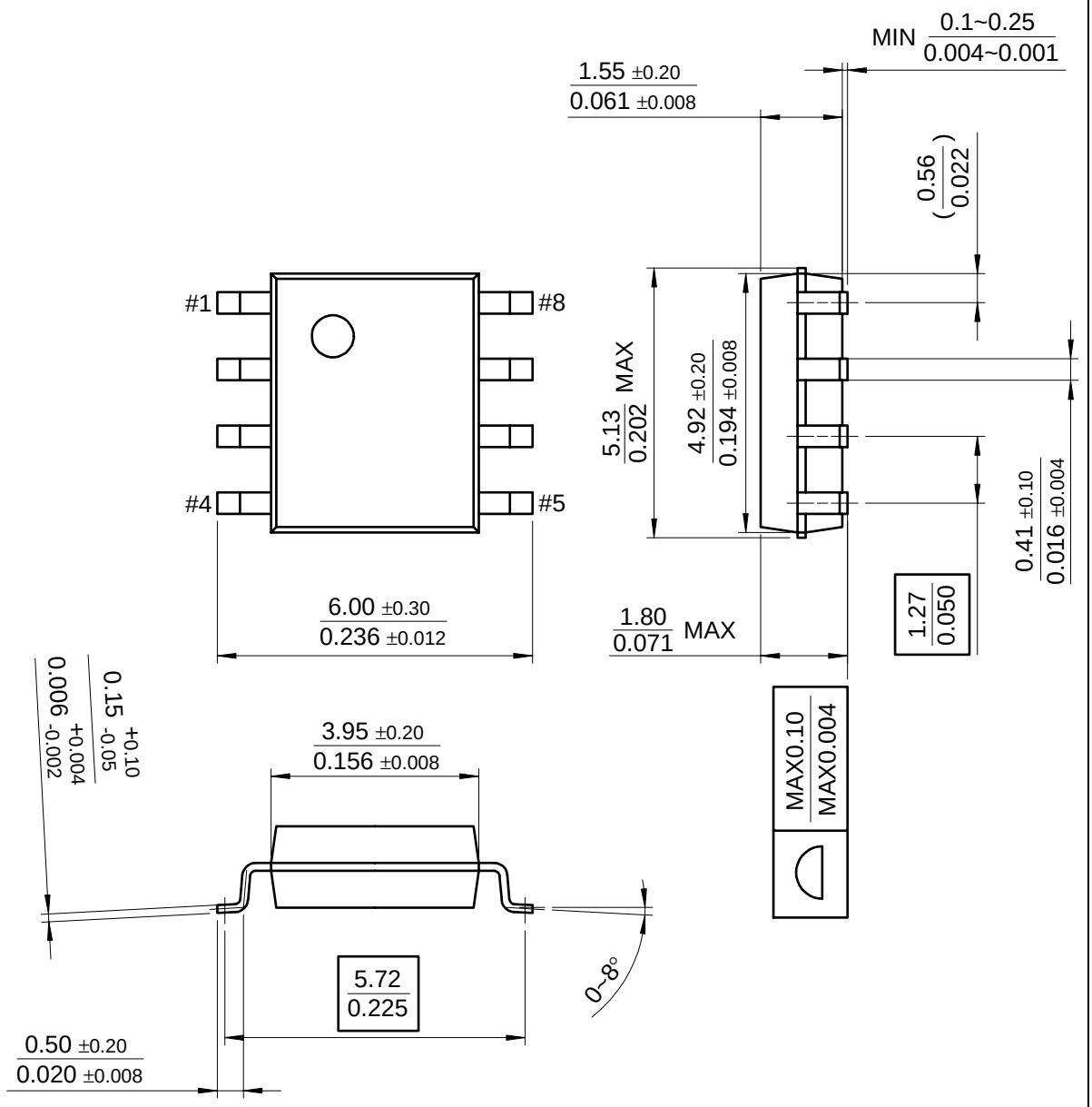






Package Dimensions

8SOP



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